Analysis of Control Strategy for Parallel Operation of Voltage Source Inverters

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Abstract - The increased inverter utilization increases the parallel operation of the inverter at grid side. The control strategy used in the inverter may fail due to another parallel inverter connected across. This paper introduces a new control strategy which is useful in parallel operation. The control system for each inverter consists of two main loops, which both use instantaneous values. The first (parallelism control) employs the feedback of the inductor current from the output filter to modify the input voltage of the same filter and, therefore, to control the power flow of each inverter to the load. Additionally, the second loop (voltage control) is responsible for controlling the output voltage of the LC filter, which coincides with the output voltage of the VSI. The proposed control strategy ensures the proper sharing of the load current and avoids current circulation among the inverters during transient and steady-state operation. Single-phase and Three-phase has been built in MATLAB/SIMULINK and its performance has been analyzed.

Keywords: Control strategy, parallelism, single-phase, Three-phase, voltage source inverters (VSIs).

I. INTRODUCTION

UNINTERRUPTIBLE power supply (UPS) systems are used to provide continuous and reliable electrical power to loads in times of unexpected power failure. By connecting the UPS inverters in parallel, its capacity is expandable. Parallel operation of inverters is gaining importance, because it increases system efficiency, provides redundancy and modularity.

Parallel operation of single phase or three phase inverters has lot of advantages, such as in cost, maintenance and reduction in size compared to single unit operated at low power.

Inverters when connected in parallel should satisfy these basic requirements:
1) Proper load current sharing between the units;
2) Should not allow current circulation between inverters;
3) Each inverter should be operated independently

Parallel connection of two or more inverters is practically difficult, because due to physical differences between the Inverter and line impedance mismatches, the load will not be properly shared which in turn leads to circulating current among them. The control techniques reported in the literature for parallel operation of inverters are centralized control, Master-slave control [1], [2], Circular Chain Control (3C) [4], [5], Active Load Sharing technique (ALS) [8],[10], Droop control method. The master-slave and central control schemes provides effective current sharing but a failure in the master or in the central unit would shut down the entire setup. The 3C and ALS scheme offers improved redundancy and modularity comparing to the previous techniques. Each inverter unit has its own parallel control system and they are connected to a common communication bus for proper sharing of data. Here a failure in the data bus would shut down the whole system. In wireless control or droop control method active and reactive power supplied to the ac bus are sensed and averaged, the resulting signals are used to adjust the voltage and frequency of the inverter reference voltage. Since this control technique does not have any control interconnection this system provides true redundancy and modularity. Each inverter operates independently and provides flexibility of connection or disconnection of an inverter at any point of connection. This control is carried out using average power values and due to the calculation of average power this method is difficult to implement.

II. CONTROL STRATEGY

The structure of a single VSI module is shown in Fig.1. Each module has its own control circuit that includes two loops. The outer loop regulates the output voltage ($V_o$) of the inverter. The inner loop is responsible for parallelism control. It uses inductor current feedback ($I_L$) from the LC filter thus modifying the output voltage ($V_{AB}$) of its own inverter which is the input voltage of the LC filter. Parallelism control uses only instantaneous values to actuate the variations of each inverter thus provides fast dynamic response to current variations. This implies that all the inverters have same output voltage since they are connected to a common ($V_{ref}$) bus. Due to parametric and component variations between the parallel inverters each inverter shows small deviations in its output voltage ($V_{AB}$). This
parallelism control which is in cascade with outer loop
equalizes the small variations between the inverters providing
proper load current sharing among the units.

The model of structure showing many VSIs in parallel
is shown in Fig. 2. All the modules are connected to a common
ac bus and a common voltage reference bus. The VSIs
connected in parallel are identical to each other. Thus the
output of the LC filter in all the units is equal. There is no
connection impedance between the inverters. Each inverter
works independently using only its instantaneous average
values. The circuit in module1 has ac-dc converter, full bridge
PWM inverter, isolation transformer and an LC filter. The
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circuit in module1 has ac-dc converter, full bridge
PWM inverter, isolation transformer and an LC filter. The
voltage control loop regulates output voltage of each inverter.
The current loop using inductor current feedback
acts on input to LC filter. The transformer provides electrical isolation.
Each inverter does not depend on the operation of other VSI
hence it is easier to connect or disconnect an inverter at any
point .the output response is not affected. The parallelism
control plays a major role in proper current sharing between
the units.

III. ANALYTICAL STUDY ON THE
CONTROL STRATEGY OF A SINGLE
INVERTER.

A. Analytical Study of the Parallelism Control

In the inverter control system, shown in module 1 of Fig. 2,
the parallelism loop obeys the control law

\[ V_{pc}(t) = V_{vc}(t) - V_i(t) \]  (1)

The parallelism control consists of subtracting a signal
proportional to the inductor \( L \) current (\( V_i \)) from the output
signal of the voltage control (\( V_{vc} \)). The signal \( V_i \) is given by

\[ V_i(t) = I_L(t) \cdot K_{IL} \]  (2)

where \( K_{IL} \) is the gain in the \( I_L \) current feedback. Replacing (3)
in (2), obtains

\[ V_{pc}(t) = V_{vc}(t) - I_L(t) \cdot K_{IL} \]  (3)

The \( V_{pc} \) signal is applied in the PWM modulator that generates
the \( V_{AB} \) voltage. It is given by

\[ V_{AB}(t) = K_{inv} \cdot V_{pc}(t) \]  (4)

where \( K_{inv} \) is the static gain of the inverter and the PWM
modulator. Since the \( K_{inv} \) gain is provided by

\[ K_{inv} = \frac{V_{dc}}{V_p} \]  (5)

where \( V_{dc} \) is the dc link voltage and \( V_p \) is the peak value of
the PWM carrier. Replacing (7) in (8), obtains

\[ V_{AB}(t) = K_{inv} \cdot V_{vc}(t) - K_{inv} \cdot K_{IL} \cdot I_L(t) \]  (6)

which it shows that instantaneous variations in \( I_L \) cause
instantaneous variations in \( V_{AB} \). Equation (6) also demonstrates the voltage droop caused by parallelism control
in the \( V_{AB} \) voltage as a function of the \( K_{IL} \) gain. Therefore,
this control can be understood as virtual resistance that is
placed in series with the \( L \) inductor, and, thus, the greater the
virtual resistance (\( K_{IL} \) gain), the higher the voltage droop with
increasing inductor current. Based on this principle, the
parallelism control consists of the proper adjustment of the \( K_{IL} \)
gain.

B. Model of One VSI With The Proposed Control Strategy

Fig. 6 shows the block diagram of the voltage and the
parallelism loops for one inverter. As the two loops have
similar dynamic responses, it is not possible to uncouple them.
Thus, the model of the inverter, which is used in the voltage loop design, must take into account the parallelism control.

![Fig. 6. Block diagram of voltage and parallelism loops for a single VSI.](image)

The model of the inverter, of the input, $V_{pc}$, to output, $I_L$, defined as $G_i(s)$, is given by

$$\frac{I_L(s)}{V_{pc}(s)} = \frac{sL \cdot \frac{1}{\tau_0}}{2L \cdot C + s(\frac{1}{\tau_0}) + 1}$$

(7)

The closed-loop transfer function of the parallelism loop, $I_{CLTF}(s)$, is shown in Fig. 6 and is considered without simplification in the model of the inverter for the voltage loop. The transfer function defines the relation between the input $I_L$ and output $V_o$.

$$\frac{V_o(s)}{I_L(s)} = G_V(s) = \frac{1}{s \cdot C + \frac{1}{\tau_0}}$$

(8)

The model of the VSI, of the input, $V_{vc}$ signal control, to the output, $V_o$ voltage considering the inverter feeding a resistive load. The voltage controller selected was the

$$C_v(s) = K C V \frac{(s+z_1)(s+z_2)}{(s+p1)s}$$

(9)

IV. SIMULATION RESULTS:

The simulation study has been carried out using MATLAB/SIMULINK.

A. Single-Phase VSI circuit and result.

Parallel operation of inverters with 5KVA and 2.5KVA was integrated with single-phase inverter. Sinusoidal PWM is used to generate pulse signal for single-phase inverter. Corresponding single-phase output voltage and current waveforms for R load of 5KW and RL load are shown in Figure 4 and Figure 5.
B. Three-Phase VSI simulation circuit and result.
Parallel operation of inverters with 5KVA and 2.5KVA was integrated with three-phase inverter. Sinusoidal PWM is used to generate pulse signal for three-phase inverter. Corresponding three-phase output voltage and current waveforms for R load of 5KW and RL load are shown in Figure 6 and Figure 7.

![Three-Phase VSI simulation circuit](image1)

![Three-Phase VSI output voltages and output currents waveforms for R load](image2)

Fig 6. Three-Phase VSI simulation circuit

Fig 7. Three-Phase VSI output voltages and output currents waveforms for R load

V. CONCLUSION:
In this paper the performance of technique for the parallel operation of VSIs single-phase and three-phase is shown. The principle of the control strategy reported herein consists of employing the feedback of the inductor current from the output filter of the VSI to modify the input voltage of the same filter. Thus, the resulting control topology utilizes only internal variables of the VSI to control its operation in the parallelism. Therefore, each inverter has its own parallelism control, which is responsible for ensuring the proper sharing of the load current and avoiding current circulation among the parallel-connected inverters. This strategy permits the parallelism of VSIs to be obtained, in which the units operate independently from each other.

REFERENCES


