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SINGLE CYCLE TREE 64 BIT BINARY COMPARATOR WITH CONSTANT DELAY LOGIC

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Abstract -In this project, Single cycle tree - based RADIX 4 stuructures 64 - bit binary comparator with constant delay logic for reducing power its realized in a 65nm techonology 1-v CMOS process is presented in this paper. This design can be done by using Tanner tool with single cycle two comparator using Priority encoder algorithm. The proposed comparator architecture are design has divided into two stage the first stage adapt noval tree comparator is specifically designed in static logic to achieve low power consumption. second stage utilizes CD logic utilizes to realize the high performance. At 1-v supply proposed comparator's measured delay is 167ps, and has and average power and a leakage power of 2.34 mW and 0.06 mW respectively.

Index Terms -Binary Comparator, Constant-Delay logic, Digital Arithmetic

[1].Introduction- Binary comparator is the one of most fundamental components in digital systems with many applications. A comparator is a device that compares two voltages or currents and switches its output to indicate which is larger. They are commonly used in devices such as analog-to-digital converters (ADCs).Dynamic logic is otherwise known as Clocked logic in some combinational logic circuits, whereas for static logic no clock is required can be paused at any time. Dynamic logic works two times faster than static logic when perfectly designed. Use of dynamic cmos in this logic circuits will perform binary comparison of large operands with high speed and area efficiency. This type of binary comparators were available in various electronic devices such as Communication systems, microprocessor, encryption devices, etc. Such high speed design takes advantage of the precharge time to compute some of the intermediate signal.

[II]Comparator Tree Design Analysis

Several 64 bit comparator tree designs are analyzed and implemented in order to determine the most energy-efficient tree structure. Variety of tree structure in a comparator is relatively less, because comparator belongs to the family of "parallel-reduction structure". Compared to a radix 2 structure, a radix 4 design reduces the number of stages by half at the expense of 2× the transistor stack height per stage.

2.1 64-Bit Binary Comparator

64-bit binary comparator compares two numbers each having 64 bits (A63 to A0 & B63 to B0). For this arrangement truth table has 128 inputs & 2128 entries. By comparing minimum number of bits, a comparator of maximum number of bits can be design using tree structure logic. Some modifications can be done in existing 64-bit binary comparator design to improve the speed . In this design, all three basic stages (0th, 1st, 2nd) have been implemented using CMOS logic style. Means stage 0^{th} of modified 64-bit comparator design have been implemented using CMOS logic style , that was implemented using modified PTL style in existing design

2.2 Radix 4

Radix-4 butterfly unit can be designed from the radix-2 butterfly structure. To design the radix-4 structure two add/sub units, four multiplexers, six registers, and multiplication by imaginary unit *j* should be added to the structure. Additional add/sub units are needed, because the number of additions and subtractions is larger, Additional registers and multiplexers are needed to implement the permutations in radix-4 butterfly operation. Multiplication by imaginary unit *j* is accomplished by a swapping of the real and imaginary parts, and negating the imaginary part.

[III].Proposed Work

3.1 Novel Comparator

Comparison between the two -bit numbers can be carried out using following array of input bits A[63:0] and B[63:0] and can be performed through an addition operation. when A[63:0] >= B[63:0] , the addition between and the 2's complement of generates a carry-out signal equal to 1, otherwise produces a zero carry-out if A[63:0] < B[63:0]. On the other hand, high-speed adders, such as the carry-lookahead adders , can drastically increase the hardware complexity, the design of efficient comparators does not usually employ addition logic. The main approach here proposed is to compare between and actually requires a special addition operation that does not produce the sum bits , only the carry-out signal is necessary to give the result. In the following, it is demonstrated how this approach makes the carry-look-ahead addition (CLA) logic useful to design high-speed comparators with reduced hardware complexity.

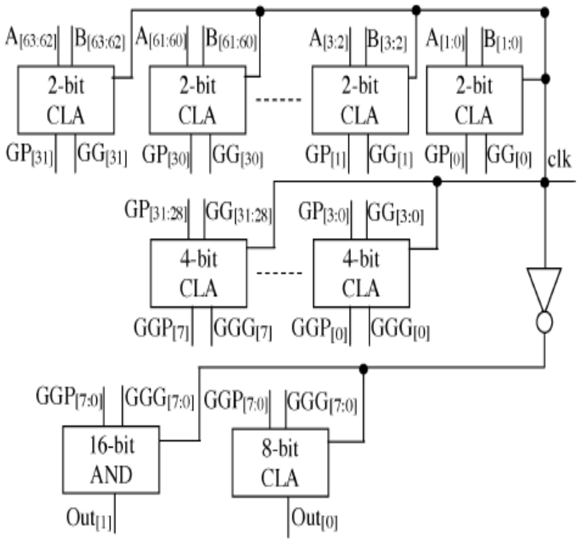
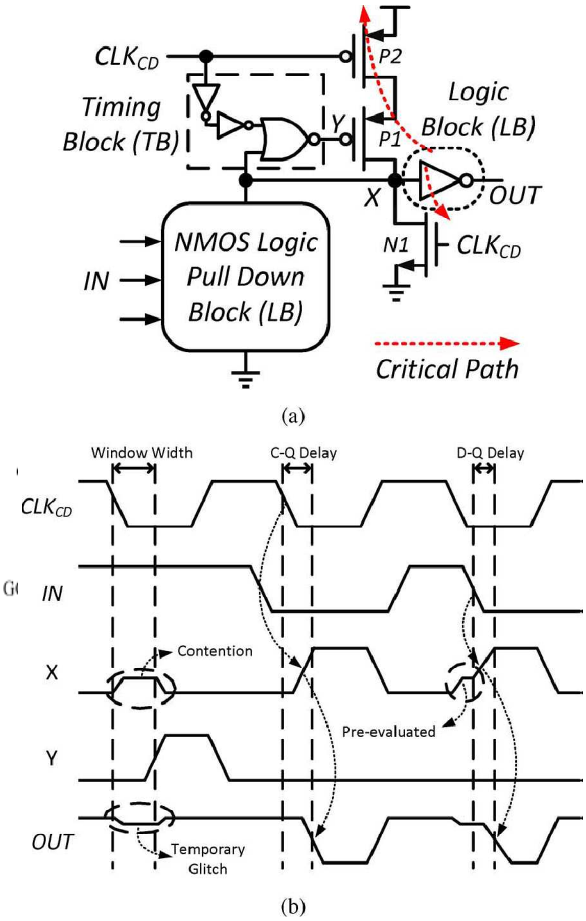


Fig: 1 64 – bit Noval Comparator

3.2 Constant Delay Logic

Constant – delay logic is realized in a 64 bit Ling adder. Timing Block(TB) creates an adjustable window period to reduce static power dissipation, While Logic Block (LB) reduces the glitch and also makes cascading CD feasiable. LB can also implement a complicated fuction, Similar to the compound domino logic, Where the output inverter of a dynamic logic gate is replaced by a more complex static gate. In CD logic style where the number of transistors required for TB. The improved CD logic reduces the transistor for TB block. This reduction helps to reduce the CD logic's overall power consumption. For a two input NAND gate, the power and area saving is approximately 5% and2 % respectively.



(a)

(b)

Fig 2 : Constant-delay (CD) Logic: (a) Block diagram and (b) Timing Waveforms.

3.3 8-Bit Comparator with CD Logic

The proposed tree-based comparator can be divided into two stages, where the first stagec consist of eight 8-bit comparators in parallel along with input signal buffers and encoding circuitries, and the second stage contains only one 8 bit comparator. This stage comparator focus on high performance even at expense of power consumption. The proposed second stage high speed 8 bit comparator architecture along with the clock generation circuit. The first stage implements a radix 2 merging with footed dynamic logic. CD logic is utilized in the second stage due to domino compatibility. 64 bit comparator acts as a high performance logic interface between dynamic and static logic.

The clock tree is arranged such that CD logic always operates in the high performance D-Q mode. First stage dynamic logic always precharge to logic “1” during the precharge period and consequently pulls down the internal node of CD logic to logic “0”. CD logic gates always operate in C-Q mode only. 8 bit comparator ,its output protected by a static inverter in case it needs to drive a long interconnect fan-ins.

3.4 Circuit Implementation

The top-level architecture of the 64-bit comparator has been proposed in fig:1, It uses three levels of operations. This condition differs from existing comparators in which the case OUT[0] and OUT [1] cannot occur. However, this does not affect the overall architecture at syste leve[8]l.

The first and second levels perform their evaluation phase when the clock signal is high, whereas they perform the precharge phase when the clock is low. The third level of the comparator operates in the opposite manner, thus making the circuit able to compare two 64-bit inputs with in only one clock cycle, the input to the eight 4-bit CLA modules of the second the 8-bit comparator of the third level completes the comparison operation as given Transistor-level implementations of the basic components used in the novel comparator are depicted It can be seen that both 4-bit and 8-bit CLA blocks exploit Manchester-Carry-Chain-based architectures. In an AMS 0.35- m implementation, nMOS transistors forming the carry chains depicted were progressively sized using a tapering factor equal to 1.5 and a minimum transistor width. Moreover, all of the precharging transistors are 1.6 m wide[8]. For all other gates, the minimum sizing approach has been used, thus making the nMOS transistors in a series m wide. Taking into account the effective loads on the signals and , the two nMOS transistors of each latch, used to correctly interface the second and third stages, are made 6 m wide, whereas a channel width equal to 4.8 m is set for the pMOS transistor. All level restorers are minimum sized .

3.5 Parallel-MSB-Checking Comparison Algorithm

A parallel MSB checking method was used instead of the priority encoding to determine the location of the Most significant bit that the two input are different. Using this method facilitates the use of NOR type logic gate and results in faster speed for dynamic logic implementation and hence results in high performance when dynamic logic is used.

A comparison function, which imposes a total ordering on some collection of objects. Comparators can be passed to a sort method (such as Collections .sort or Arrays .sort) to allow precise control over the sort order. Comparators can also be used to control the order of certain data structures (such as sorted sets or sorted maps), or to provide an ordering for collections of objects that don't have a natural ordering.

3.6 64-Bit Tree Based Comparator

Pre-encode circuitry. 64-bit comparator is here designed in 7 stages. In the 0th stage, modified pass transistor logic style circuitry is employed to produce “less than” & “equal to” outputs. The outputs of 0th stage act as inputs of 1st stage. In 1st stage, CMOS circuitry is employed to produce inverse inputs for stage 2nd. In 2nd stage, CMOS circuitry is employed again to produce actual inputs for stage 3rd. Now, according to tree structure given in Fig. 1, circuitry of first stage is used for third stage. Similarly, for fourth stage, circuitry of second stage is employed. For the fifth stage first stage circuitry is employed. For sixth stage the second stage circuitry employed.

The size of the comparator grows larger, the third- and even the fourth-level look-ahead circuit structures, which are similar to that used in the priority encoder can be used to shorten the critical path further. However, not only does the structure of a single gate become more complex, but also the propagation delay grows linearly to the number of the cascading macros in [4]. Therefore, for a longer comparator, we propose a twos tage pipelined structure to enhance the performance with little increase.

The previous design approach needs a precharge phase and an evaluation phase to finish one comparison operation. Thus, the precharging time is wasted from the viewpoint of logic operation. Furthermore, the duty cycle of a system clock is usually set to be 50% despite that the required precharging time is typically shorter than the evaluation time. Taking these factors into consideration, we partition the logic functions of the comparator into each half of the clock cycle to form a two-stage pipeline. Such a design not only makes each pipeline shorter but also fully utilizes the clock cycle if the circuit is implemented in the dynamic CMOS logic. When the first pipeline stage enters the evaluation phase, the second pipeline stage enters the precharge phase. After the first pipeline stage turns to precharge and latches the results, the second pipeline stage begins to evaluate. Although the new architecture needs more transistors for pipeline latches, it can effectively shorten the clock cycle to improve the operating speed. Furthermore, implementing the circuit by dynamic CMOS circuits, the comparator can still finish each comparison in one clock cycle.

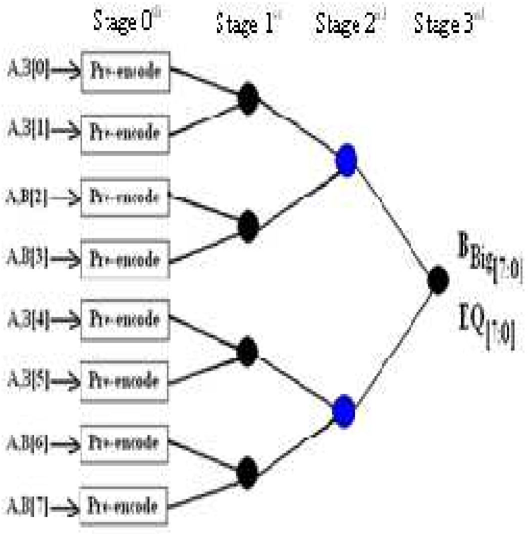


Fig :3 Tree Diagram Of 8-Bit Comparator

The 64 input bits are partitioned into eight small groups, each having eight input bits. In the first pipeline stage, eight comparators process eight groups of inputs respectively, producing eight pairs of outputs and . After latching, these outputs are sent to the second stage, which is another 8-bit comparator, to perform the rest operations. A comparison function, which imposes a total ordering on some collection of objects.

[IV]Performance Parameters Of Design

4.1 Power Dissipation

Power dissipation is a measure of the power consumed by the logic gate when fully driven by all its input. The D.C or average power dissipation is the product of D.C supply voltage and the mean current taken from the supply. We can compute the whole power dissipation through the following equation-

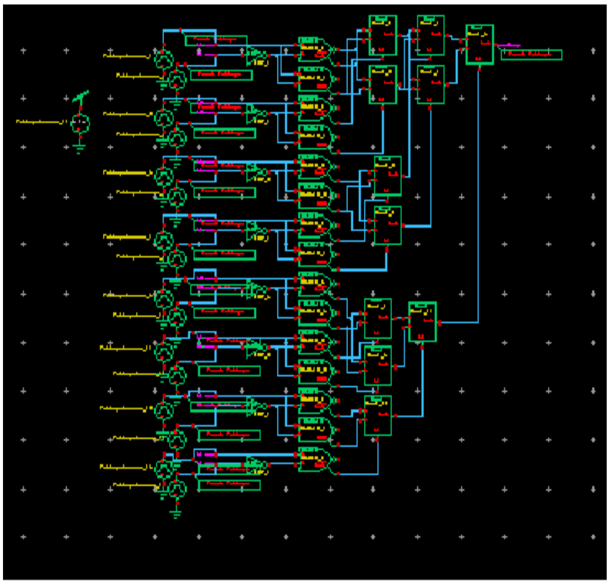
P total = P static + P dynamic + P short cir
P = α CL Vdd2 fclk(Isc + I leakage)Vdd

4.2 Propagation Delay

The propagation delay can be defined as time required to reach 0.5 Vdd of output from the 0.5 Vdd of input. The propagation delays of Carry look ahead adders are measured in orders of nanometers. This is the important factor in CLA design. The propagation delay of carry bit is calculated. The speed of adder is depending upon propagation delay how fast circuit is work

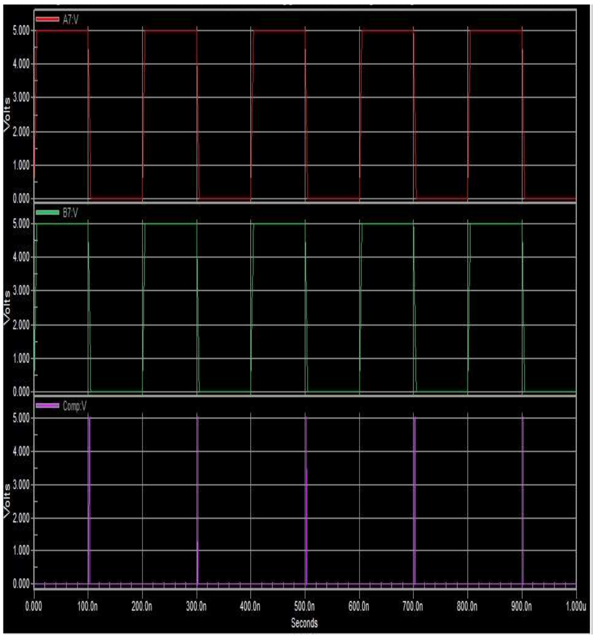
[V].Simulation and Results:

5.1 Circuit Diagram:



8-Bit Comparator

4.2Output Waveform:



[V].CONCLUSION

5.1 CONCLUSION

A new high-performance logic style with CD characteristic and self-reset circuitry was proposed. The pre-evaluated feature of CD logic makes it particularly suitable in a circuit block where a unique critical path exists and performance is the primary concern. We have suggested an idea of designing an 8 – bit CLA using tanner tool and simulated an output waveform corresponding to the input patterns assigned to reduce the power as wells as the number of transistor stages in an 64 – bit binary comparator using radix -4 structure as a result delay time have been reduced 2.63 seconds.. CD logic is 20% faster or 17% more energy-efficient than the proposed comparator with static logic only, respectively.

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