Behavioral Analysis of Three stage Interleaved Synchronous DC-DC Converter for VRM Applications

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Abstract—Multiphase interleaving Synchronous DC - DC Converter is widely used for voltage regulator modules (VRMs) which requires strictly steady and dynamic performances to power microprocessor. For feasible and effective ripple reduction, proper designing the air gap and coupling coefficient is needed if the correct magnetic topology is used that greatly improves the efficiency of the VRM. For more than two phases, this can be a “ladder” core with windings around each rung. Typical ripple reduction is better than a factor of six with no effect on response time. One can also chose to improve response time while still significantly reducing ripple. MATLAB simulation of Four phase VRM show that coupled inductor can improve dynamic performance.

Key Words - Synchronous Buck Converter, Multiphase, Ladder, Transient response, filter Inductor, trade-off, phase current, ripple current.

I. INTRODUCTION

It is predicted that the future microprocessors demand more and more power and at the same time the required voltage levels continue to drop. In future, voltage go below 1V and current will go beyond 120A[1]. To handle this huge current multiphase interleaving technology is preferred. In non isolated Voltage Regulator Module (VRM), lower voltage, higher current and fast transient response is required to supply microprocessors[2]. The multiphase interleaving technology helps to reduce the current ripples at the output and improves the transient response [3]-[5]. The challenge is that the load current can change from near zero to full load or vice versa in nanoseconds and the voltage has to be maintained constant throughout. The combination of high current and fast response requires a voltage regulator module (VRM) located immediately adjacent to the load. The VRM must be small in size as well as have high efficiency and extremely fast response.

At present, the standard design used for high-performance VRMs is a buck converter with multiple parallel sections, staggered in phase [6], [7]. In a buck converter with a load-current step, the output capacitor supplies (or sinks) the immediate difference in current while the inductor current is ramped up or down to match the new load current. A small inductor allows ramping the current quickly to minimize the output capacitor requirement. However, small inductor values also lead to large ripple current. In a single-phase converter, large ripple current in the inductor increases the output capacitor requirement when the inductor is very small [7]. The standard multiphase interleaved design avoids this problem because it achieves substantial ripple current cancellation in the output capacitor [8]. This allows smaller inductance without requiring a large output capacitor. However, the full ripple current flows through the MOSFET switches (including synchronous rectifiers) and through the inductor itself, resulting in higher losses and higher peak current requirements. One strategy to reduce the ripple current throughout is to operate at very high switching frequencies but this increases switching and gate-drive losses and imposes difficult requirements for magnetic materials capable of low loss at very high frequencies.

Fig. 1. shows the general schematic diagram of an n phase coupled buck converter which is most common in today’s VRM topologies.

![Fig. 1. Interleaved Multi-phase Buck DC-DC converter](image-url)
II. LIMITATIONS OF MULTIPHASE BUCK CONVERTER

A. DUTY CYCLE INFLUENCE ON RIPPLE CANCELLATION

One of the important advantages of multiphase buck converter is the effect of ripple cancellation that enables the use of small inductance to improve the transient response and to minimize the requirement of output capacitance.

In the of multiphase buck converter, the inductor current ripples in the individual phases are cancelled at the output and the total ripple current flowing into the output capacitor is reduced. With the cancellation of ripple at the output, the output voltage ripple becomes very small. A small inductance can be used to improve the transient response, and hence a small output capacitance can be used to meet the transient requirements.

For the multiphase buck converter, the magnitude of the output current ripples is given as

\[ \Delta I_L = \frac{V_o (1-D)}{L_o f_{sw}} \]  

(1)

Where \( L_o \) is the inductor per phase, \( f_{sw} \) is the switching frequency.

![Fig. 2. Effect of Duty Cycle on Ripple Cancellation](image)

Fig. 2. shows the influence of duty cycle on output current ripple. The output current ripple is normalized against the inductor current ripple at zero duty cycle.

Fig. 2. shows that with a very small duty cycle, the current ripple cancellation is poor in the multiphase buck converter. Thus the advantage of the multiphase buck converter as far as using a small inductance to improve the transient response is compromised.

B. INFLUENCE OF DUTY CYCLE ON EFFICIENCY.

In the multiphase buck converter, a small duty cycle results in large current ripples in the inductors, that increases the conduction and switching losses of MOSFETs, and also the losses in the inductors.

Fig. 3 shows the measured efficiencies for a four-phase synchronous buck converter for two different input voltages, 5 V and 12 V. The output voltage, output current and switching frequency are 1.5 V, 50 A, and 300 kHz, respectively. The measured efficiency data include the power losses in the power stage, but exclude the control and gate drive losses.

As can be seen from Fig. 3, for 5 V input, the multiphase buck converter can achieve 87% efficiency at full load and 91% peak efficiency, while for 12 V input, the multiphase buck converter can only reach 81% efficiency at full load and 84.5% peak efficiency. With the increase of input voltage from 5 V to 12 V, the duty cycle is decreased from about 0.3 to 0.125. The decrease of the duty cycle reduces the full-load efficiency by about 6% and peak efficiency by about 7%. This efficiency drop is mainly caused by the increased switching loss in the control MOSFETs.

![Fig. 3. Efficiency of four-phase buck converter](image)

III. TRADEOFF BETWEEN EFFICIENCY AND TRANSIENT RESPONSE.

One of the most important issues with VRM is the selection of output LC filter parameters. Generally, for VRMs, this selection is based on the output-voltage ripple specification, but on the tradeoff between the specified VRM efficiency and transient response.

To summarize, the efficiency of the multiphase buck converter suffers from a very small duty cycle, mainly due to the increased switching loss in the main MOSFETs.
The minimum capacitance which is required to keep the transient output voltage within the regulation limits, can be estimated using the approach presented in [9]. Assuming that the VRM control responds immediately to the load change, i.e., assuming that the control-loop bandwidth is infinite, the buck converter equivalent circuits during the load step-up and step-down transients are shown in Fig. 2(a) and (b), respectively. From Fig. 4(a) and (b), the rate of the inductor current change is

\[
\frac{dI_L}{dt} = \frac{V_{IN} - V_o}{L_F} \quad \text{during step up transient (2a)}
\]

and

\[
\frac{dI_L}{dt} = \frac{-V_o}{L_F} \quad \text{during step-down transient (2b)}
\]

According to (2a) and (2b), for a 12-V/1.5-V VRM, the rate of inductor current change is much higher during a step-up than during a step-down transient because input voltage \(V_{IN}\) is much higher than output voltage \(V_o\). Therefore, the output-voltage overshoot during a load step-down transient sets the limit on the VRM transient performance [10].

Where \(V_{IN}\) is input voltage

\(V_o\) is output voltage

\(L_F\) is filter inductor.

To keep VRM output voltage \(V_o\) within regulation range \(\Delta V_o\) during a load transient of magnitude \(\Delta\), the minimum required output-filter capacitance is

\[
C_{FMIN} = \frac{1}{2} \frac{\Delta V_{MAX}}{\Delta V_o} \left( \frac{L_F}{V_o} - \frac{1}{\frac{dI_o}{dt}} \right) \quad (3)
\]

where \(\frac{dI_o}{dt}\) is the load-current slew rate.

According to equation (3), output-filter inductance \(L_F\) has to be minimized to achieve a fast transient response with the minimum output capacitance. However, a low inductance value increases the inductor current ripple, which has a detrimental effect on the VRM efficiency. Not only increased inductor-current ripple increases conduction losses due to the increased rms currents, but more importantly it dramatically increases the buck switch turn-off loss due to the increased peak value of the inductor current. The detrimental effect of a high inductor-current ripple on the VRM efficiency is illustrated in Fig. 3 which shows the measured efficiency of a 12-V/1.5-V, 20-A single-phase VRM as a function of the switching frequency for different values of the output-filter inductance. As can be seen in Fig. 3, at any switching frequency the VRM efficiency decreases as the output-filter inductance decreases from 470 nH to 160 nH. Generally, the efficiency drop is more pronounced at lower switching frequencies, i.e., below 300 kHz. Specifically, at 200 kHz the efficiency drop is 5.5% when the inductance is reduced from 470 nH to 250 nH, whereas the efficiency drop when inductance is reduced from 250 nH to 160 nH is around 10%. However, at \(f_s = 700\) kHz, for example, the corresponding efficiency drops are only 4% and 2%.

Fig. 5 also shows that for a given output-filter inductance value there is an optimal switching frequency at which the VRM efficiency is maximized. For a large output-filter inductance, e.g., \(L_F = 470\) nH, the efficiency monotonically increases as the switching frequency decreases. The improvement of the efficiency at lower frequency is caused by reduced switching losses, in particular, the turn-off switching loss of the buck switch. However, for lower values of the output-filter inductance, i.e., for \(L_F = 250\) nH and \(L_F = 160\) nH, the maximum efficiency does not occur at the minimum switching frequency. In fact, for \(L_F = 250\) nH, the maximum efficiency occurs at \(f_s = 300\) kHz, whereas for \(L_F = 160\) nH, the optimal switching frequency is in the 400–550 kHz range. The efficiency
decrease at low frequencies for low output-inductance values is caused by the increased turn-off switching loss of the buck switch because of the increased peak inductor current.

The reduction of the output-filter inductance without penalizing the conversion efficiency can be achieved by employing the interleaving approach. Since for an interleaved converter the output-filter inductors of the individual modules are effectively connected in parallel, the transient response of the interleaved converter is governed by effective inductance

\[ L_{\text{EFF}} = \frac{L_F}{N} \]  

where \( N \) is a number of interleaved phases. Consequently, in an interleaved converter, the desired transient response can be achieved with a smaller output-filter capacitance than in a single-module converter [10].

Optimization of the VRM efficiency and transient performance requires careful selection of the switching devices, switching frequency, output-filter components, and number of interleaved modules. Selection of the buck switch and SR devices is driven by their operating conditions. Since SR conducts the inductor current for the most of the switching cycle, its conduction loss is considerably higher than that of the buck switch. At the same time, the SR switching loss is minimal because, by proper selection of delays between the buck switch and SR gating signals, SR can be turned on and off with zero voltage across it. Therefore, it is desirable to select the device with the lowest on-resistance for SR. However, for the buck switch, it is crucial to select the device with the lowest turn-off loss that is determined by many parameters such as the device fall time, gate charge, internal gate resistance, and package parasitic inductance [11].

After the switching devices are chosen, the next design step is to select inductance \( L_F \) and the module switching frequency which correspond to the specified VRM efficiency. The analytical tool for \( L_F \) value selection was proposed in [10]. However, practical design optimization can be most efficiently performed empirically, using a single--phase prototype circuit. The data similar to that shown in Fig. 4 is helpful in determination of the optimal switching frequency.

The final design step is to estimate the minimum amount of the output capacitance which satisfies the transient spec. If the estimated \( C_F \) value is unacceptable, the effective inductance \( L_{\text{EFF}} \) has to be decreased by increasing the number of interleaved phases.

### IV. DESIGN CONSIDERATIONS.

Generally, multiphase VRMs are designed to supply high current at very low output voltage so as to take care of high power dissipation at very high current levels.

For designing a practical converter, we need to take into account the various parasitic effects of the components involved. Following is the design specification for multiphase VRM:
- Input Voltage, \( V_d = 12\text{V} \)
- Output Voltage, \( V_o = 0.8\text{V} \)
- Load Current, \( I_o = 90\text{A} \) (so load resistor \( R=8.88\text{m}\Omega \))
- Switching Frequency, \( f_s = 400\text{kHz} \)
- Duty Ratio, \( D = 0.066 \)
- Peak-Peak ripple current is limited to 30% of load current, so \( \Delta I = 27\text{A} \)

#### A. Calculation for Inductor.

For steady state operation, the change in current is given by

\[ \Delta I = \frac{(V_{IN} - V_{O})D\tau_s}{L} = \frac{(V_{O})(1-D)\tau_s}{L} \]  

By rearranging equation (5), we can find the value of the inductor as,

\[ L = \frac{(V_{IN} - V_{O})D\tau_s}{\Delta I} \]  

Solving equation (6) we get \( L = 70\text{nH} \).

#### B. Calculation of Output Capacitor

The voltage ripple across the output capacitor is the sum of ripple voltages due to the “Effective Series resistance” (“ESR”), the voltage sag due to the load current that must be supplied by the capacitor as the inductor is discharged, and the voltage ripple due to the capacitor’s ESL or “Effective Series Inductance”. It is given by:

\[ \Delta V_o = \Delta I \cdot \left(ESR + \frac{\Delta T}{c} + \frac{ESL}{\Delta T}\right) \]  

As the ESL specification is usually not specified by the capacitor vendor so the ESL value is assumed to be zero. At very high switching frequencies (>1 MHz), the ESL specification becomes more important. Simplifying equation (7) by assuming \( ESL = 0 \):

\[ \Delta V = \Delta I \cdot (ESR + \frac{\Delta T}{c}) \]  

Rearranging, we get
The acceptable output voltage ripple, $\Delta V_{o}$, is defined as 5mV and ESR is selected as 0.03 $\Omega$. Solving equation (9) with $\Delta V_{o} = 5$ mV, $\Delta I = 0.3$ A, ESR = 0.03 $\Omega$, and $\Delta T = (0.066 / 400$ kHz) = 165ns, yields the value of capacitor as $C = 12$ $\mu F$. Power loss in the capacitor is given by: $(\text{ripple})^2 \times \text{ESR}$.

\[ C = \frac{(\Delta I \times \Delta T)}{(\Delta V - (\Delta I \times \text{ESR})} \]  

(9)

V. SIMULATION RESULTS
To verify the design, simulation is carried out in the Matlab/Simulink environment. Fig. 6. shows the simulink model of 3 stage synchronous DC-DC Converter.

Fig. 6. Simulink model of 3 stage Synchronous DC-DC Converter.

Fig.7. shows phase currents of 3-phase interleaved synchronous DC-DC converter and per-phase ripple current for k= 1 and f=400kHz.

Fig. 7. Phase current and ripple current waveform of 3phase Synchronous DC-DC Converter.

From fig. 7. it is observed that for the designed filter inductor value, as frequency increases, ripple current cancellation is better with tight coupling. This reduces losses per phase and the overall efficiency of the VRM increases. It is also observed that transient response is good at higher switching frequency.

Fig. 8. shows output voltage and output current waveform of 3-phase synchronous DC-DC converter. From fig. 8. it is observed that output voltage do fairly confirm the desired output voltage of 0.8V and output current is 90A.

By increasing the value of filter inductor we can reduce the ripple, as well as we are able to achieve desired value of output voltage and current.

Fig. 8. Output voltage and output current of 4-phase Synchronous DC-DC Converter.

Fig. 9. shows the phase currents and phase ripple current with reduced value of switching frequency for K=1. and switching frequency of 50kHz.

Fig. 9. . Phase current and ripple current waveform of 3-phase Synchronous DC-DC Converter for k=1, f=50kHz

From Fig. 9., we can observe that the phase current ripple is high. It is also seen that as switching frequency decreases current ripple increases leading to more losses which in turn reduces the efficiency of the converter. The transient response is fairly same as in case of 400kHz.

Fig.10. shows the output voltage and output current waveform.
**TABLE 1.**

<table>
<thead>
<tr>
<th>Switching Frequency in kHz</th>
<th>Ripple Current in Amp</th>
<th>Settling time in msec</th>
<th>Ripple Current in Amp</th>
<th>Settling time in msec</th>
<th>Ripple Current in Amp</th>
<th>Settling time in msec</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>0.6</td>
<td>0.1</td>
<td>0.31</td>
<td>0.25</td>
<td>0.2</td>
<td>0.4</td>
</tr>
<tr>
<td>200</td>
<td>0.15</td>
<td>0.2</td>
<td>0.08</td>
<td>0.30</td>
<td>0.06</td>
<td>0.5</td>
</tr>
<tr>
<td>400</td>
<td>0.08</td>
<td>0.2</td>
<td>0.04</td>
<td>0.35</td>
<td>0.03</td>
<td>0.5</td>
</tr>
</tbody>
</table>

Table 1. shows the ripple current and transient responses for different coupling coefficients and various switching frequencies.

Figure 12 shows as switching frequency and coupling coefficient increases, transient time increases. It is always preferred to have lower settling time. If settling time increases, transient losses also increase. Hence, to achieve desired efficiency and transient response, we need to optimally choose switching frequency, filter components and coupling coefficient.

**V. CONCLUSION**

Design considerations for the 12V/0.8V, 90A multiphase interleaved synchronous DC-DC converter for VRM applications were presented. It is observed that for all switching frequencies and coupling coefficients output voltage and output current remains constant at 0.77V and 88A respectively. The VRM power-stage design which can meet the specified efficiency and transient requirements was discussed. The limits of multistage VRM applications were demonstrated.

**VI. REFERENCES**
