Critical-Path Analysis and Low-Complexity Implementation of the LMS Adaptive Algorithm

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Abstract—The filter process mainly used in DSP and DIP real world application. The filter process is to remove the noise in original signal or image. So the filter architecture optimized process is to reduce the filter processing time and to increase the performance. Adaptive digital filters find wide application in several digital signal processing (DSP) areas. The ASIC based technology to modify the filter architecture level. The filter architecture mainly focused by the addition process and to optimize the carry selection time. So we use the carry save adder architecture. The filter architecture to increase the system speed and to improve the system performance level. The distributed based RAM design is proposed to the FPGA architecture. In this architecture, the proposed method used to design DA based FIR filter architecture. This paper presents the modified delayed LMS adaptive filter consists of Weight update block with Partial Product Generator (PPG) to achieve a lower adaptation delay and efficient area, power, delay. To achieve lower adaptation delay, initially the transpose form LMS adaptive filter is designed but the output contains large delay due to its inner product process. Here, the pipelining structure is proposed across the time consuming combinational blocks of the structure to reduce the critical path. From the simulation results, we find that the proposed design offers large efficient output comprises the existing output with large complexities. We use the digital architecture based VLSI technology to modify the FIR filter architecture. In this architecture, we use a novel partial product generator and to modify the efficient architecture for the implementation of a delayed mean square adaptive filter using FIR algorithm. This DA-based FIR filter architecture is to develop the VHDL language using XILINX 14.2 software.

Index Terms—FIR Filter, LMS algorithm, least mean square adaptive filter

I. INTRODUCTION

Very-large-scale integration (VLSI) is the process of creating integrated circuits by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductors and communication technologies were being developed. Before the introduction of VLSI technology most ICs had a limited set of functions they could perform. An electronics circuits might consist of a central processing unit to Read only memory, Random access memory and other Glue logic. VLSI lets IC makers add all of these into one chip.

Structured VLSI design is a modular methodology originated by Carver Mead and Lynn Conway for saving microchip area by minimizing the interconnect fabrics area. This is obtained by repetitive arrangement of rectangular macro blocks which can be interconnected using wiring by abutment. An example is partitioning the layout of an adder into a row of equal bit slices cells. In complex designs this structuring may be achieved by hierarchical nesting.

Structured VLSI design had been popular in the early 1980s, but lost its popularity later because of the advent of placement and routing tools wasting a lot of area by routing, which is tolerated because of the progress of Moore's Law. When introducing the hardware description language KARL in the mid 1970s, Reiner Hartenstein coined the term “structured VLSI design” (originally as “structured LSI design”), echoing Edsger Dijkstra’s structured programming approach by procedure nesting to avoid chaotic spaghetti-structured programs.

It has been seen that only 40% power is reduced in case of the adaptive filter when compared to decimation filter. We have so far concentrated mainly on algorithmic approach of power reduction. Now we proceed to integrate both circuit level and algorithmic level power reduction technique to apply to our problem of hearing aid design. In this chapter we focus on FIR filter which is the primary component of hearing aid design. Here in this design FDF (Folded Direct Form) of FIR filter structure is adopted. We have additionally focused on the clocking strategy to reduce glitches that facilitates power reduction; a novel circuit for latch is also proposed. This clocking strategy in conjunction with the latch is adapted for the FIR filter structure that is used for hearing aid.

II. LEAST MEAN SQUARE ADAPTIVE FILTERS

The Least Mean Square adaptive filter is the most popular and most widely used adaptive filter, not only because of its simplicity but also because of its satisfactory convergence performance. The direct-form LMS adaptive filter involves a long critical path due to an inner-product computation to obtain the filter output. The critical path is required to be reduced by pipelined implementation when it exceeds the desired sample
period. Since the conventional LMS algorithm does not support pipelined implementation because of its recursive behavior, it is modified to a form called the delayed LMS (DLMS) algorithm, which allows pipelined implementation of the filter.

A lot of work has been done to implement the DLMS algorithm in systolic architectures to increase the maximum usable frequency but, they involve an adaptation delay of N cycles for filter length N, which is quite high for large order filters. Since the convergence performance degrades considerably for a large adaptation delay, have proposed a modified systolic architecture to reduce the adaptation delay. A transpose-form LMS adaptive filter is suggested, where the filter output at any instant depends on the delayed versions of weights and the number of delays in weights varies from 1 to N. Van and Feng have proposed a systolic architecture, where they have used relatively large processing elements (PEs) for achieving a lower adaptation delay with the critical path of one MAC operation.

In this design filter coefficients are loaded in bit-parallel form with no increase in the number of input pins, thereby facilitating and speeding up run-time adaptation to the application environment. This type of design methods can be applied for the design of application- specific and embedded parallel architectures.

III. LITERATURE SURVEY

R. Rocher, D. Menard, O. Sentieys, and P. Scalart Proposed the implementation of adaptive filters with fixed-point arithmetic requires to evaluate the computation quality. The accuracy may be determined by calculating the global quantization noise power in the system output. In this paper, a new model for evaluating analytically the global noise power in the LMS algorithm and in the NLMS algorithm is developed. Two existing models are presented, then the model is detailed and compared with the ones before. The accuracy of this model is analyzed by simulations. A global model must be developed for this term. Nevertheless, further studies have to be carried out in order to develop this methodology for all types of systems and particularly, nonlinear systems. The truncation is the most common mode used in embedded systems. Indeed, its implementation requires no additional hardware[17].

Kyo Takahashi, Naoki Honma and Yoshitaka Tsuneka [20] proposed a Distributed Arithmetic (DA) is an efficient calculation method of an inner product of constant vectors, and it has been used in the DCT realization. Furthermore, it is suitable for time varying coefficient vector in the adaptive filter. The new algorithm and effective architecture of the MDA-ADF are discussed. The objectives are improvements of the MDA-ADF permitting the increase of an amount of hardware and power dissipation. The convergence properties of the new algorithm are evaluated by computer simulations, and the efficiency of the proposed VLSI architecture is evaluated. The two elements of DWAFS are updated, simultaneously the timing chart of the SMDA-ADF. The parallel computation of the output calculation and update procedure are realized by the delayed update method.

Yuen-Hong Alvin Ho, Chi-Un Lei and Ngai Wong [21] proposed a novel common-sub expression-elimination (CSE) algorithm that models synthesis of coefficients into an estimated cost function. Although the proposed algorithm generally does not guarantee an optimum solution, it is capable of finding the minimum/minimum of the function in practically sized problems. In our design examples that have known optimal solutions, syntheses of coefficients using the proposed method match the optimal results in a defined search space. We also discover the relationship and propose an improvement search space for optimization that combines all minimal-signed-digit (MSD) representations as well as the shifted sum (difference) of coefficients to explore the hidden relationship. In some cases, the proposed feasible solution space further reduces the number of adders/subtractors in the synthesis of MCM from all MSD representations. They have also proposed an expansion of differential coefficient solution space that generally further reduces the number of adders in the synthesis of MCM from all MSD representations, which reduces power consumption and silicon area in circuit.

Gowri.T, Rekha.M [17] here the Filters are used for digital signal processing applications like filtering operations. Various forms of filters like Direct form, transposed form and cascaded form. They are specific building blocks to construct the Finite Impulse Response (FIR) filter, to achieve the desired frequency response. FIR filter design allow hardware optimization, that can not affect the filter operation and output signal. According to this adders, registers and multipliers are the resources to be optimized, conventional or classical or traditional FIR filters have performance degradation in area, delay and power dissipation. A technology named as MCMAT (Multiple Constant Multiplication Accumulation and truncation) in direct FIR structure is proposed for FIR filter design. It utilizes resource efficient multipliers namely truncated multipliers for performance improvement strategy. The design of FIR Filter structure using Multiple Constant Multiplication Accumulation and Truncation (MCMAT), which lead to smallest area and low power consumption. The simulation and synthesis result show that, the power consumption is 3195.57mw using 121 taps. By using MCMAT in direct form, the Performance factor such as area and power are reduced compare to MCM and MCMA.

R Krishnapriya, D Rukmanidevi [18] proposed an efficient architecture design technique for the implementation of delayed least mean square adaptive filter, for achieving lower adaptation-delay and efficient area-delay-power implementation. We use a novel partial product generator and propose a strategy for optimized balanced pipelining across the time-consuming combinational blocks of the structure. The structure of each PPG consists of L/2 number of 2-to-3 decoders and the same number of AND/OR cells (AOC). The normal LMS algorithm does not support pipelined implementation because of its recursive behavior; it is
modified to a form called the delayed LMS (DLMS) algorithm. Aside from this, a strategy for optimized balanced pipelining across the time consuming blocks of the structure to reduce the adaptation delay and power consumption, as well. The proposed structure involved significantly less adaptation delay and provided significant saving of ADP and EDP compared to the existing structures. Fixed-point implementation of the proposed architecture, and derived the expression for steady state error.

IV PROBLEMS IDENTIFIED

- In reality, to be sure that the coefficients do not diverge, a limit of $0.6\mu_{\text{max}}$ is chosen.
- The adaptive filters have proven to be useful in these environments of multiple input/output, variant-time behaviors, and long and complex transfer functions effectively, but fundamentally they still have to evolve.
- LDB is the predefined logic depth bound that limits the maximum logic depth of the MCM.
- The Total Power dissipation is high.
- Existing does not reduce the hardware complexity without noticeable degradation.

V PROPOSED WORK

The existing system consists more add and multiply operators and consumes more power, accuracy to be low and the path delay also increased. The system performance is too low. The Proposed system used to the FIR digital filter architecture for the digital image processing application and to modify the area for FIR filter architecture

(A) Pre-Processing

The input bit to be applying the delay circuit. The shift process to add the pre-processing section. At the same time the error bit to apply the delay unit section. The error bit to be applying the co-efficient block and go the next DA-based PPG block. Then the input is sequentially apply to the modified partial protect generation circuit.

(B) Partial Protect Generation

The modified partial protect generation to be apply the input signal and the error signal. The DA-based carry save adder architecture used to the PPG addition process. The modified PPG circuit used to modify fixed point LMS adaptive algorithm. The proposed fixed point LMS algorithm to apply the modified PPG architecture. It is used to reduce the pattern count for PPG circuit.

(C) Shift-Add Architecture

The modified PPG circuit output to be given to the multiplier architecture. The reduced multiply operator using shift-add tree method. This method used to optimize the multiplier gate count. So reduce the power consumption level. To perform the entire operations for getting the final product, the conventional architecture for shift and add multipliers require many switching activities. The PPG circuit output to be given to the multiplier architecture. The multiply operator using shift-add tree method. This method used to optimize the multiplier gate count. So reduce the power consumption level.

(E) Delay-Adder Unit

The reduced delay-adder unit to be apply the input for shift-add architecture. The delay unit to apply sequentially in this operation. So the final output to be produced and we using the fixed point LMS adaptive algorithm to reduce the delay circuit and to improve the efficiency of proposed system. This filter architecture to reduce the power consumption level and to improve the carry selection processing DA-based filter architecture.

The least-mean-square (LMS) is a search algorithm in which a simplification of the gradient vector computation is made possible by appropriately modifying the objective function. The LMS algorithm, as well as others related to it, is widely used in various applications of adaptive filtering due to its computational simplicity. The convergence characteristics of the LMS algorithm
are examined in order to establish a range for the convergence factor that will guarantee stability. The convergence speed of the LMS is shown to be dependent on the Eigen value spread of the input signal correlation matrix. In this chapter, several properties of the LMS algorithm are discussed including the misadjustment in stationary and nonstationary environments and tracking performance. The analysis results are verified by a large number of simulation examples. This analyzing the finite-word length effects complements this.

VII RESULTS

The ISim GUI opens and loads the design. The simulator time remains at 0 ns until you specify a run time. For comparison purposes, you can browse to the completed folder for a completed version of the simulate_isim.bat batch file.

Fig. 2 Simulation Graph

Fig. 3 RTL Diagram

Fig. 4 Technology Diagram

(A) Performance Comparison
VIII CONCLUSION

In this project the main objective is to reduce an area–delay–power efficient low adaptation delay architecture for fixed-point implementation of LMS adaptive filter. We used a novel PPG for efficient implementation of general multiplications and inner-product computation by common sub expression sharing. Besides, we have proposed an efficient addition scheme for inner-product computation to reduce the adaptation delay significantly in order to achieve faster convergence performance and to reduce the critical path to support high input-sampling rates. Aside from this, we proposed a strategy for optimized balanced pipelining across the time-consuming blocks of the structure to reduce the adaptation delay and power consumption, as well. The proposed structure involved significantly less adaptation delay and provided significant saving of ADP and EDP compared to the existing structures.

The highest sampling rate that could be supported by the ASIC implementation of the proposed design. When the adaptive filter is required to be operated at a lower sampling rate, one can use the proposed design with a clock slower than the maximum usable frequency and a lower operating voltage to reduce the power consumption further.

REFERENCES