Design and Implementation of Square and Cube Architectures using Vedic Sutras on FPGA

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Abstract— This paper describes the design and implementation of binary square and cube architectures using Vedic sutras. Square and cube are arithmetic operations which forms the heart of the different DSP operations like Image Compression, Decoding, Demodulation, Least Mean Squaring etc. Traditionally squaring and cubing were performed using conventional multipliers which consumes more area and results in large delay. Therefore Vedic mathematics properties are exploited here to reduce the delay and to improve the area. In this work binary squaring architecture is designed using properties of Dwandwa yoga sutra and this architecture is improved further. Binary cubing is designed using Anurupyena sutra of Vedic mathematics. These architectures achieve better area in terms of slices and reduce combinational path delay. Comparison is made between conventional and Vedic methods. Synthesis is done on Xilinx FPGA Device using, Xilinx Family: Spartan 3, speed grade -5.

Keywords:; Anurupyena, Cube, Dwandwa yoga, Square, Vedic mathematics.

I.INTRODUCTIOIN

Squaring and cubing are most important arithmetic operations having wide applications in different areas of engineering and technology [1].Square and cube of a number can be calculated using multipliers. Perhaps these are the most time consuming operations in implementing large hardware circuitry. Performance of a circuit mainly depends on silicon area and delay. Hence, dedicated square and cube hardware may significantly improve the silicon area and reduce the delay to large extent.

Vedic mathematics is an ancient system of mathematics. This was re-discovered by Sri Bharathi Krishna Tirthaji between 1911 and 1918 [2].There are sixteen sutras and thirteen sub sutras in Vedic mathematics. These sutras cover almost every branch of mathematics. Application of sutras minimizes lots of time and effort in solving problems, compared to formal methods. This paper proposes a possible application of Vedic mathematics to design squaring and cubing circuits for binary numbers.

Urdhava Tiryakbyam sutra of Vedic mathematics is used for implementing Vedic multiplier. Partial product generation and additions are done concurrently in Vedic multiplier. This feature makes it more efficient than array and booth multiplier in terms of execution speed [3],[4]. Four bit binary number squaring using Vedic multiplier and duplex property is described in [5]. According to this work, Vedic mathematical method is computationally faster and easy to perform than conventional methods. But this method is applied only for four bit numbers. As number of bits increases proposed method in [5] becomes complex. Anurupyna sutra of Vedic mathematics [2] is used to find cube of a decimal number, but not applied for binary number.

This work attempts to design and implement square and cube architectures for eight bit binary numbers using Vedic mathematics properties. Main goal is to reduce the delay and to achieve better area in terms of slices.

II.SQUARE ARCHITECTURE

The Dwandwa yoga sutra which is also known as ‘duplex combination’ is used for finding square of a decimal number. Duplex ‘D’ of any number is the sum of square of the middle number and two times the product of the other pairs. For example

\[ D(a) = a^2 \]
\[ D(ab) = 2ab \]
\[ D(abc) = 2ac+b^2 \]
\[ D(abcd) = 2ae+2bd+c^2 \]

Square of a two digit number using Duplex property is given by

\[ (ab)^2 = D(a)|D(ab)|D(b) \]

Example:

\[ (24)^2 = D(2) \mid D(24) \mid D(4) \]
D (4) = 4^2 = 16 = 6 = A
D (24) = 2 * 2 * 4 = 16 + 1 = 17 = 7 = B
D (2) = 2^2 = 4 + 1 = 5 = C

Now the required result after squaring is CBA = 576.

A. 8-Bit Square Architecture using Duplex property

The block diagram of 8-bit squaring circuit using Duplex property of Dwandwa yoga sutra is shown in Fig. 1. This architecture consists of two 4-bit squaring circuits, one 4*4 Vedic multiplier and two adders. In order to add three numbers at a time, carry save adder is used as first adder. And carry-look ahead adder is used as second adder because of its less delay.

Block diagram of 2*2 Vedic multiplier which is used to design 4*4 Vedic multiplier is shown in fig 3. It requires four input AND gates and two half-adders.

1) 4*4 Vedic multiplier

Block diagram of 4*4 bit Vedic multiplier using Urdhava Tiryakbyam sutra is shown in fig 2. To get final product, four 2*2 bit Vedic multipliers and three four bit ripple-carry adders are required. To reduce the hardware overhead ripple carry adders are used. And arrangements of RC adders help to reduce delay [4].

2) 4-Bit Vedic Squaring circuit

4-bit Vedic Squaring circuit requires one 2*2 Vedic multiplier, two 2bit Vedic squaring circuits, 4 bit carry save adder and 4 bit carry-look ahead adder. 2 bit Vedic squaring circuit is nothing but 2 * 2 bit Vedic multiplier. 4-bit Vedic squaring architecture using Duplex property of Dwandwa yoga sutra is shown in fig 4.
III. CUBE ARCHITECTURE

Cube of two digit decimal number can be calculated by using Anurupena sutra of Vedic mathematics.

Example:

\[ 24^3 = 2^3 | 2^2*4 | 4^2*2 | 4^3 \]

<table>
<thead>
<tr>
<th></th>
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<th>8</th>
<th>16</th>
<th>32</th>
<th>64</th>
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<tbody>
<tr>
<td>8</td>
<td>16</td>
<td>3</td>
<td>32*3</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>48</td>
<td>96</td>
<td>64</td>
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Now add them up with carry over excess digits from right to left.

\[ 8+5=13 \ | 48+10=58=8 \ | 96+6=102=2 \ | 4 \]

\[ 24^3 = 13824 \]

Architecture to find cube of 8-bit binary is designed using the concept of Anurupena sutra. This architecture requires two 4-bit cubing circuits which can be designed using same architecture as proposed here for 8 bit. 16-bit carry-save adder is used to add three 16-bit numbers at a time. And one 4-bit ripple-carry adder is used to add remaining bits so as to obtain last two bits of final output.
IV. RESULTS

In this work, 8-bit squaring and cubing architectures are implemented in Verilog HDL. Simulation is done in Xilinx ISE 12.2 simulator. Figure 7 to 9 shows the simulation waveforms of Dwandwa yoga squaring circuit, improved squaring circuit and cubing circuit for various possible input combinations. Area and combinational path delays of proposed squaring and cubing are compared with conventional methods. Comparison is shown in Table 1,2. Tabulated results shows that Vedic methods are better compared to conventional methods in terms of area and delay.

V. CONCLUSION

Due to regular and parallel structure of Vedic square and cube, it can be concluded that these are faster than conventional square and cube. Because of reduced hardware complexity and delay the proposed square and cube can be implemented in Arithmetic and Logic Units replacing the traditional square and cube circuits. Improved squaring circuit can be used for DSP and cryptography applications which involve time consuming square operations. Proposed designs can be extended for higher number of bits of unsigned numbers. Future scope of research is to reduce power requirements.

REFERENCES